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APPROVED BY DRAFTSMAN	O.G. FIG. 4	SUBCLASS
	CLASS 7/4	794

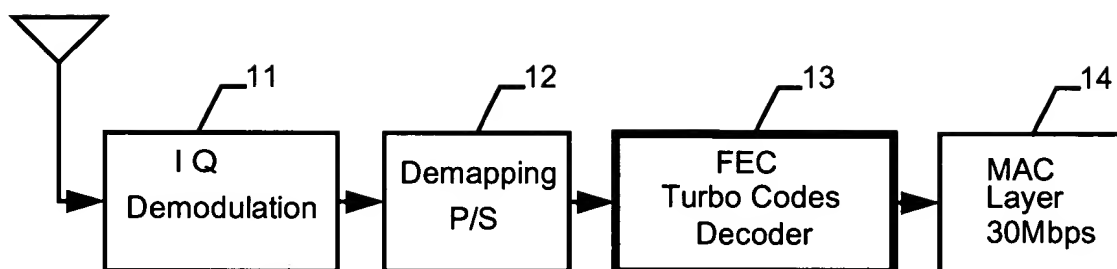
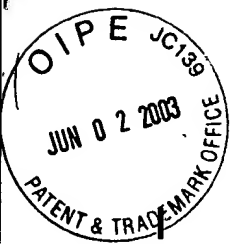


FIGURE 1. Typical 3G Receiver Functional Block Diagram, (Prior art)



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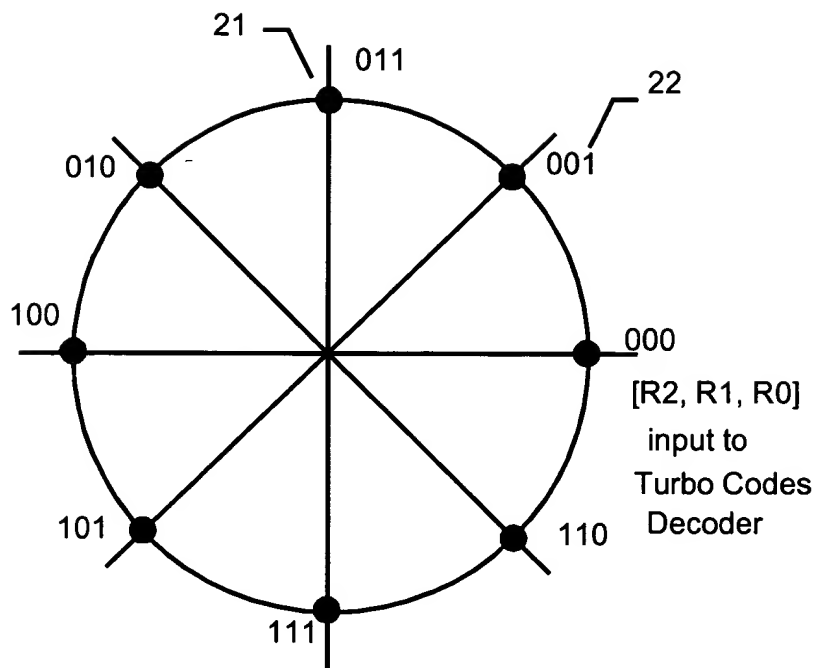
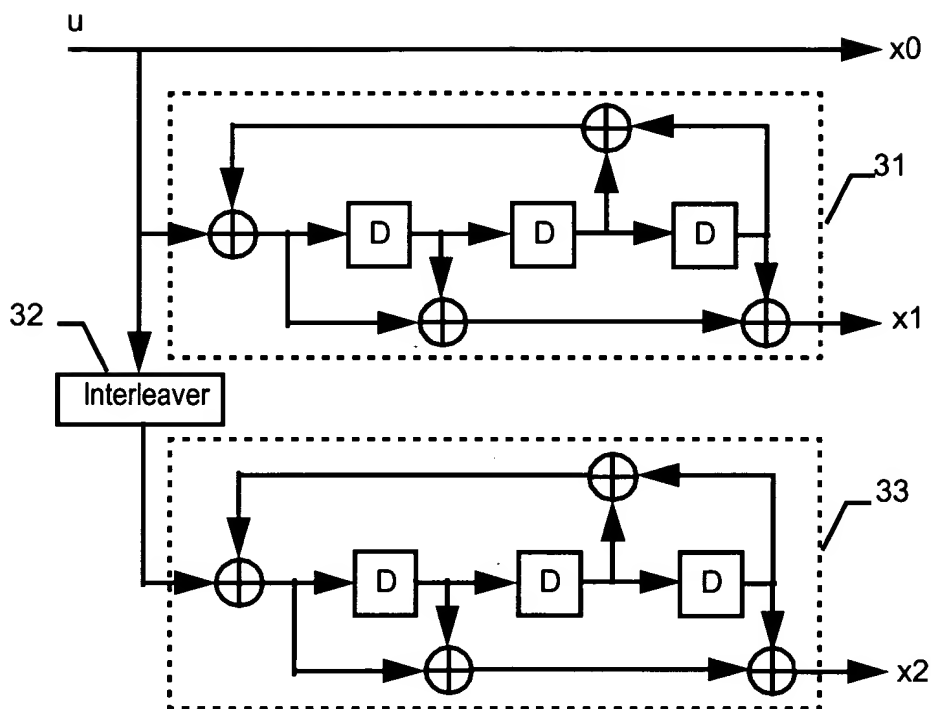


FIGURE 2. 8-PSK constellations, (Prior art)

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$$G(D) = [1, n(D) / d(D)]$$

where, $d(D) = 1 + D^2 + D^3$, $n(D) = 1 + D + D^3$

FIGURE 3. The 8-states Parallel Concatenated Convolutional Code (PCCC)
(Prior art)

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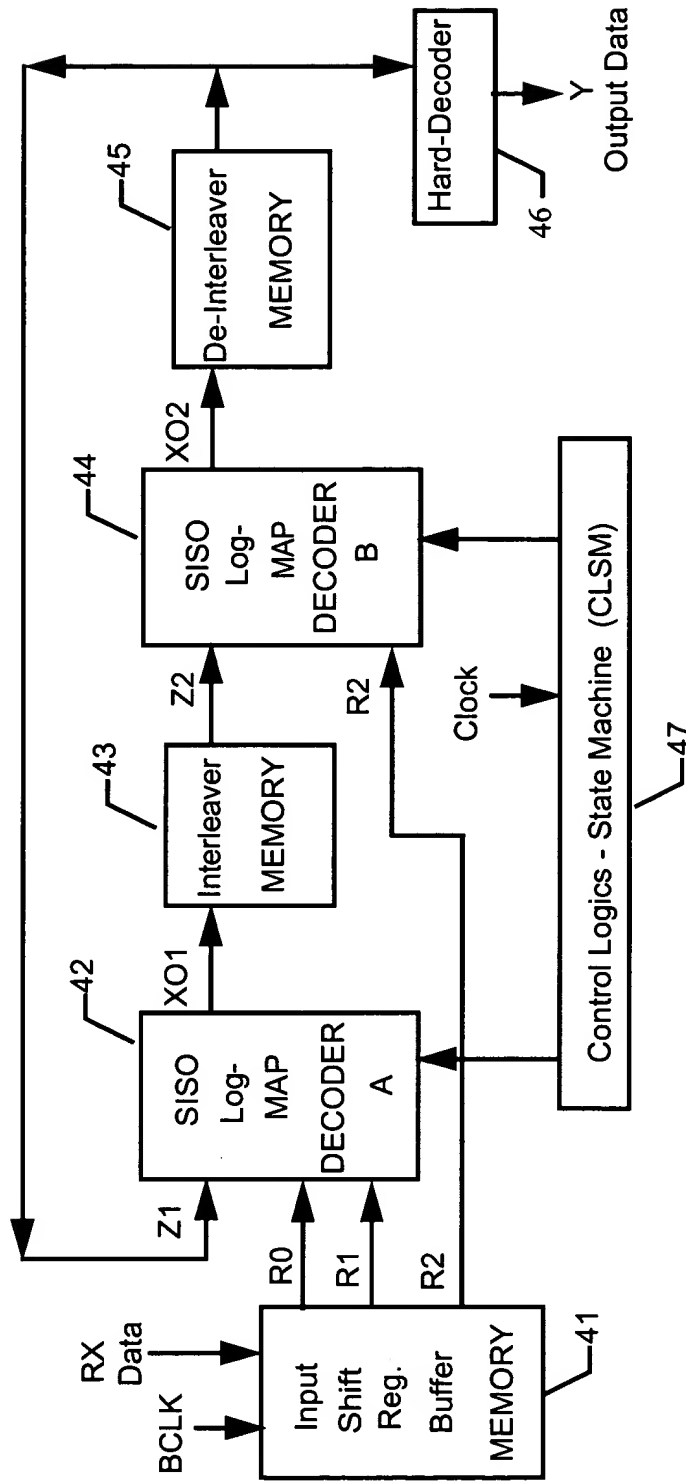


FIGURE 4. Turbo Codes Decoder System Block Diagram

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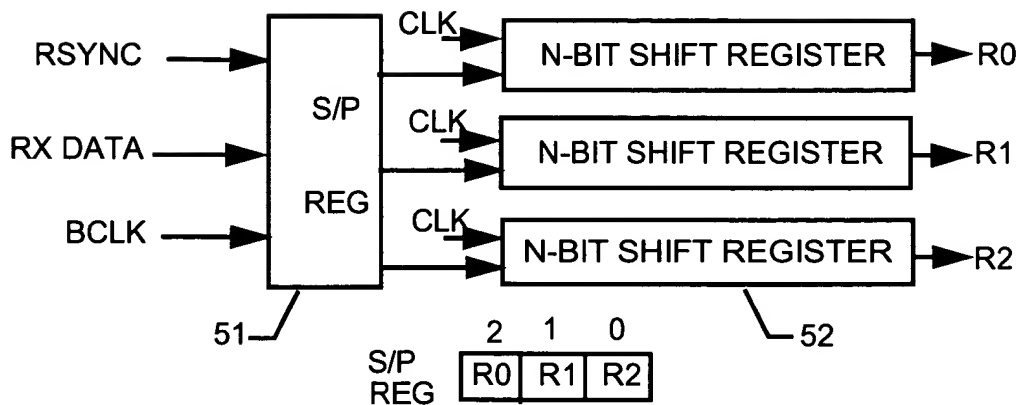


FIGURE 5. Input Buffer Shift Registers



FIGURE 5b. Soft Values Mapping ROM Table

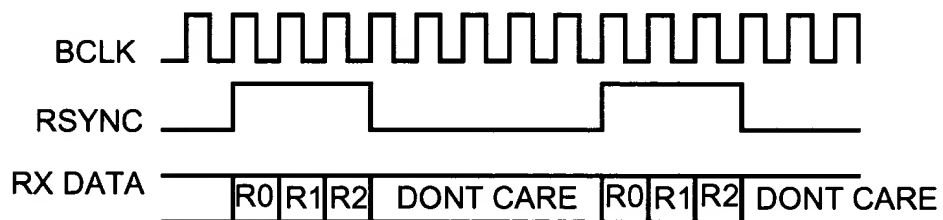


FIGURE 6. Input Buffer Interface Timing

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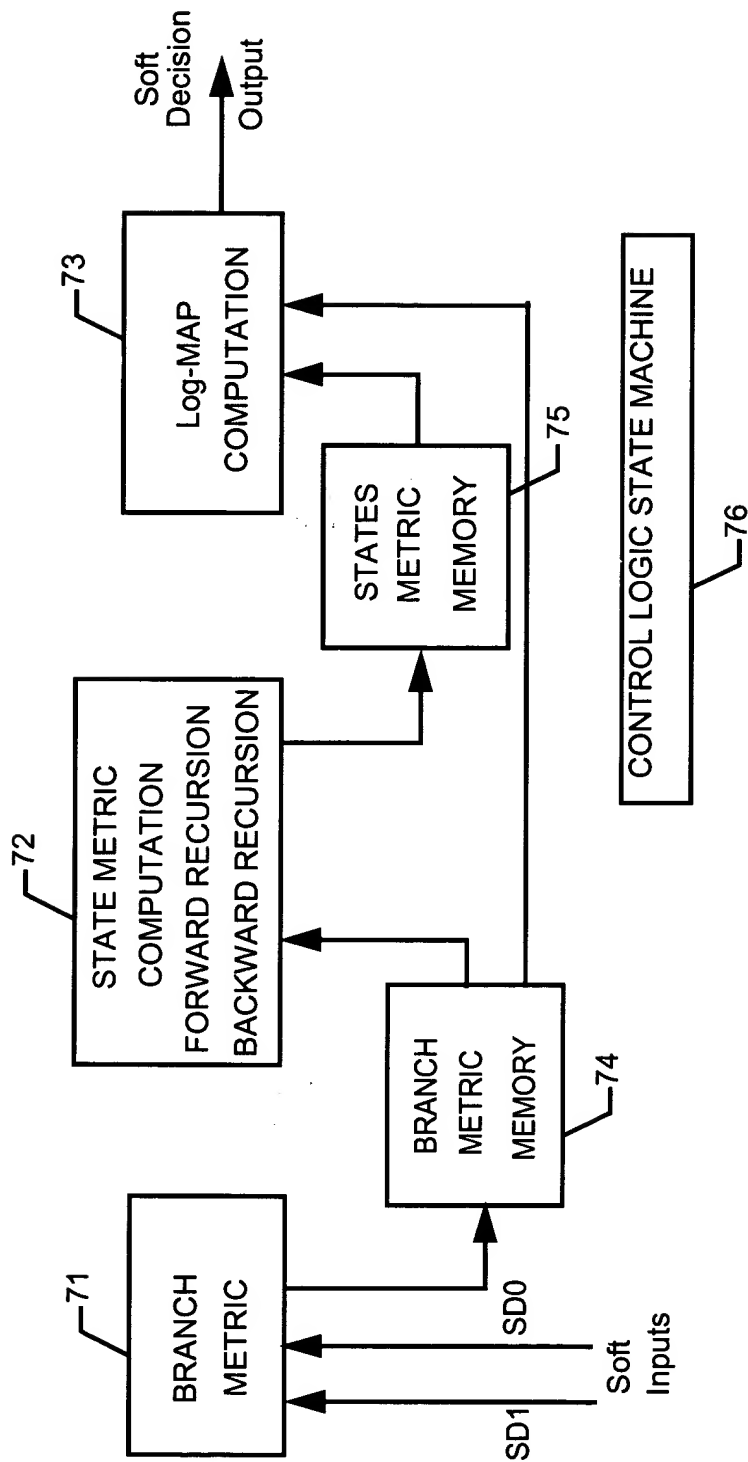


FIGURE 7. The 8-states SISO Log-MAP Decoder

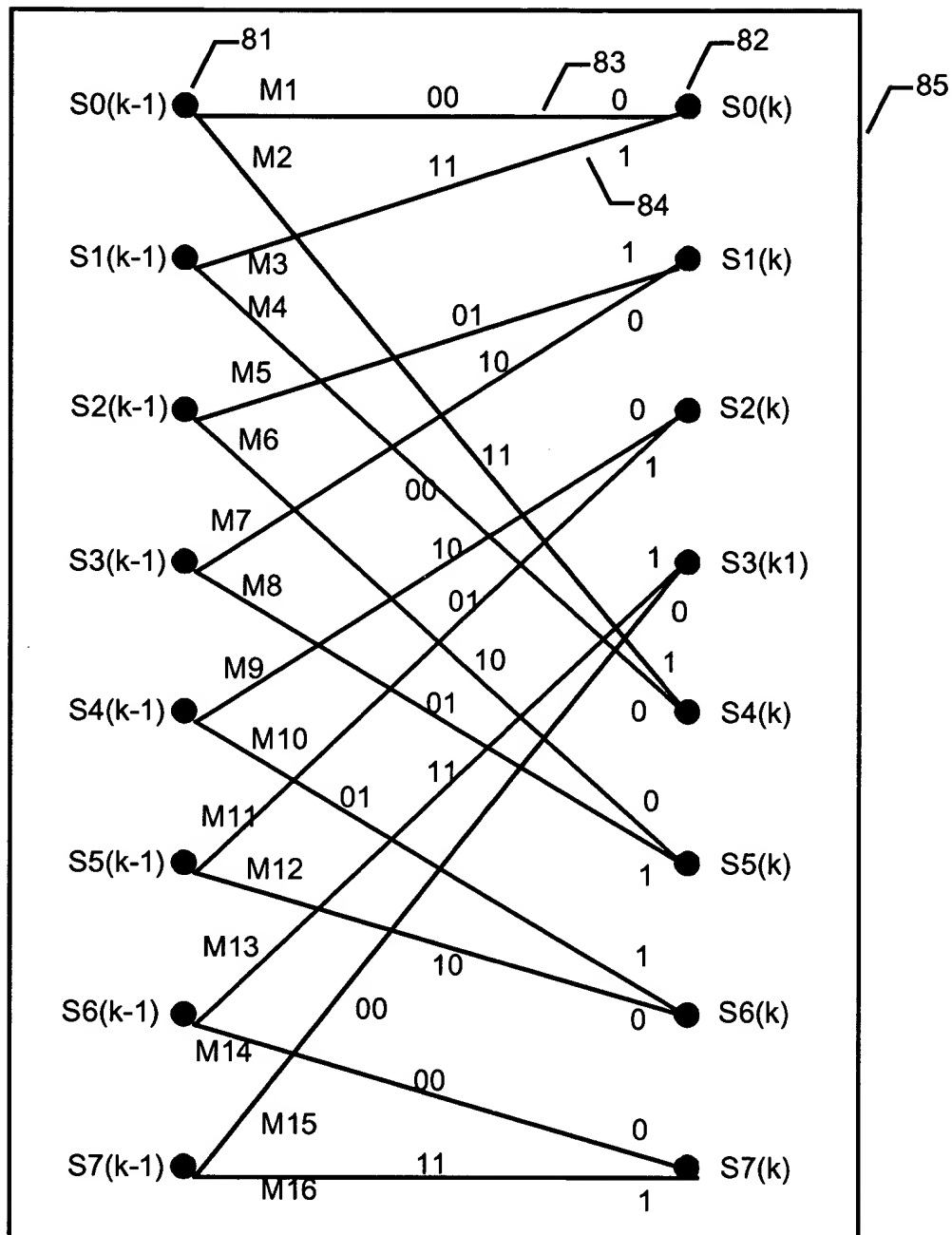


FIGURE 8. The 8-STATES TRELLIS DIAGRAM of a SISO Log-MAP Decoder

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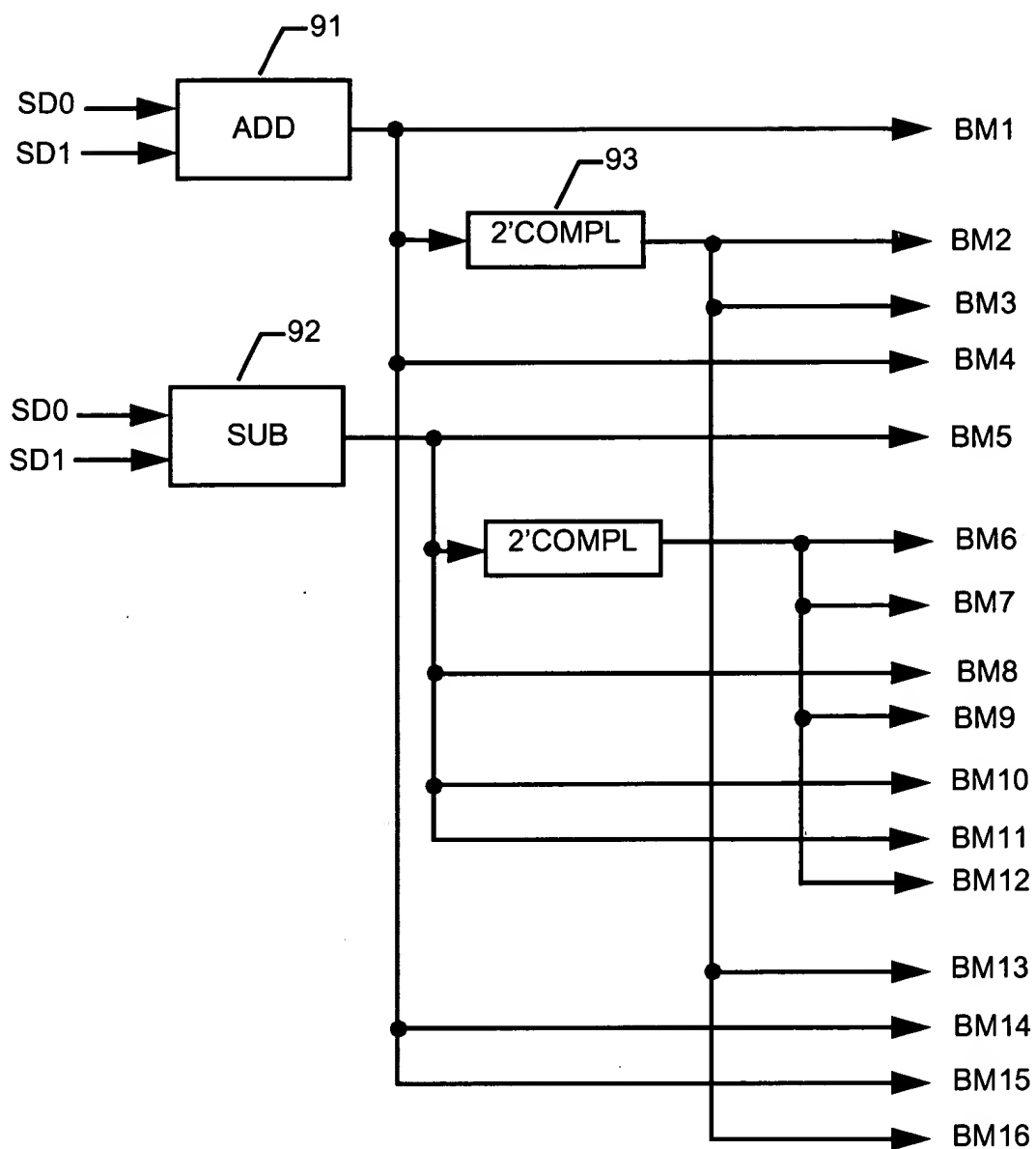


FIGURE 9. BRANCH METRIC COMPUTING MODULE

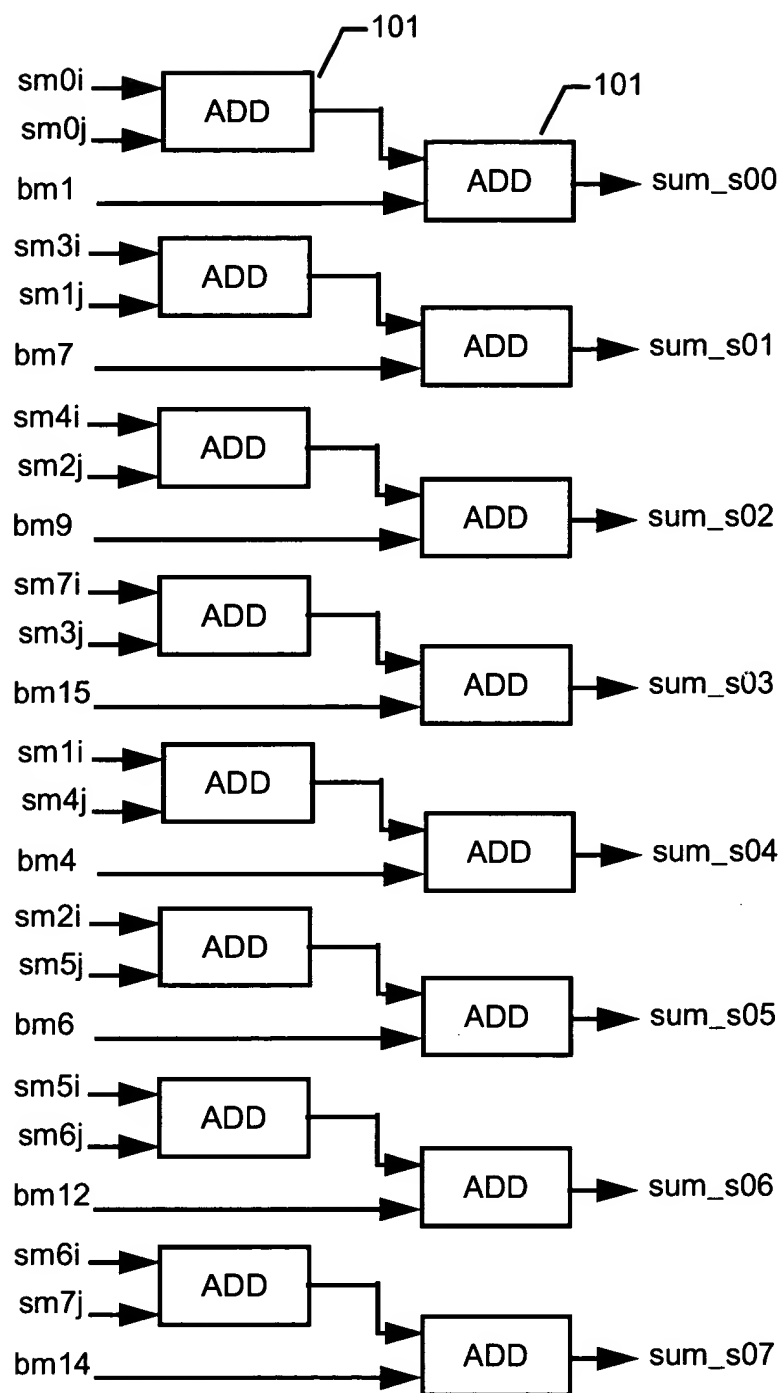
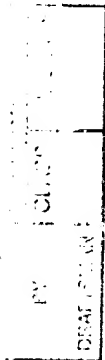
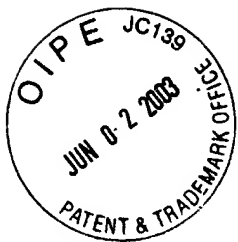


FIGURE 10a. LOG-MAP COMPUTING MODULE



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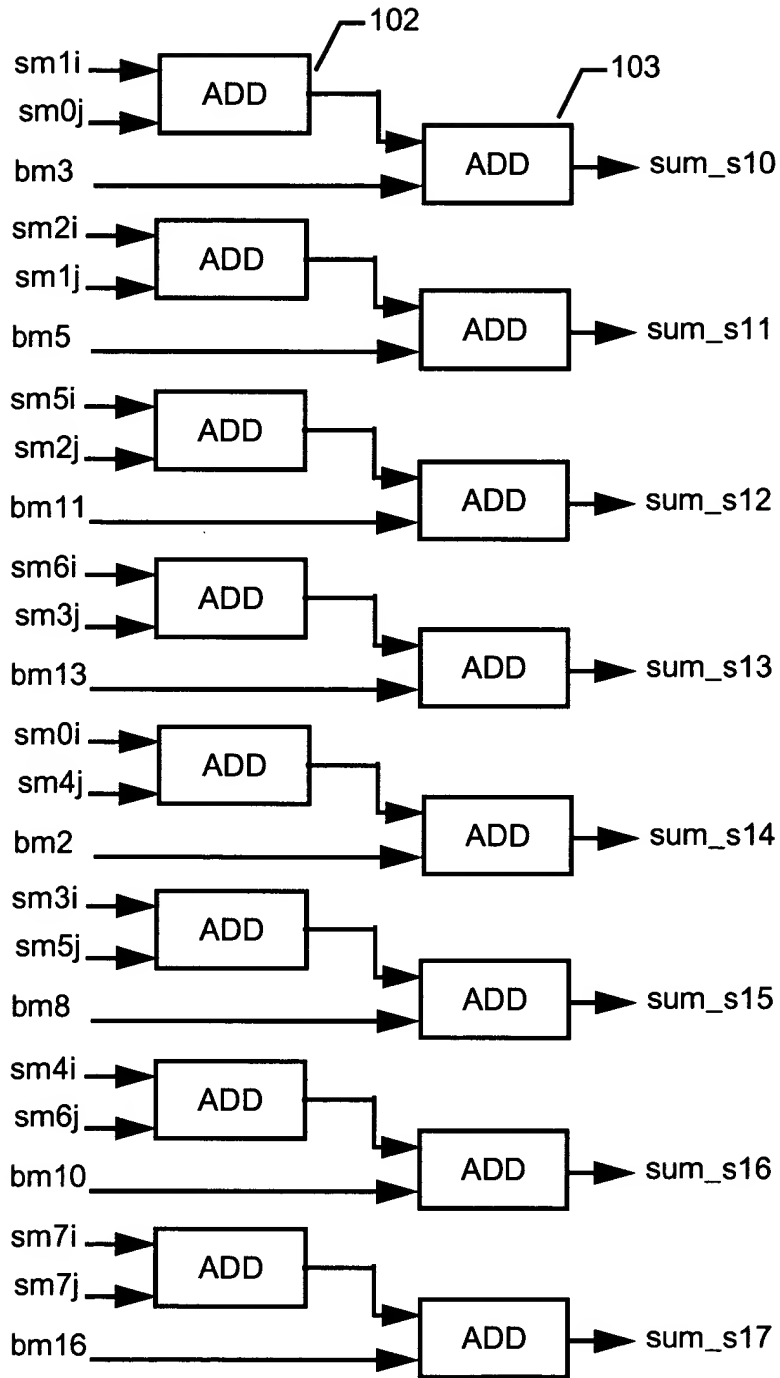


FIGURE 10b. LOG-MAP COMPUTING MODULE

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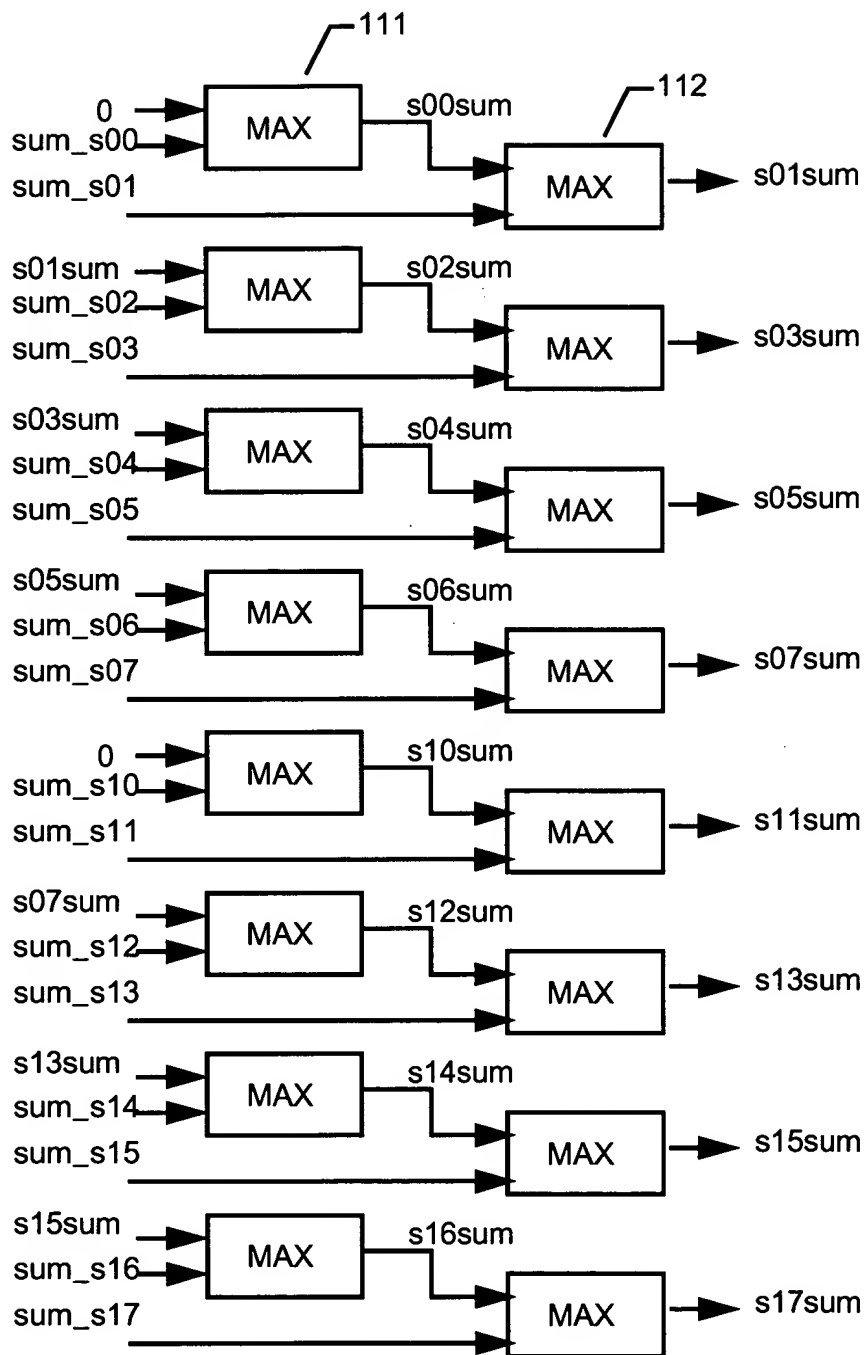
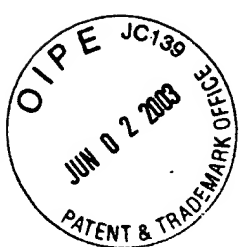


FIGURE 11. Computing Log-MAP for each state



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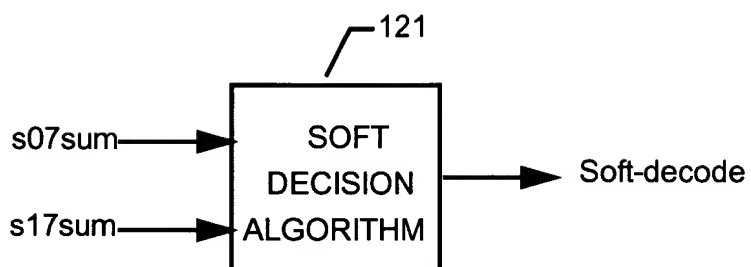


FIGURE 12. Soft Decode output



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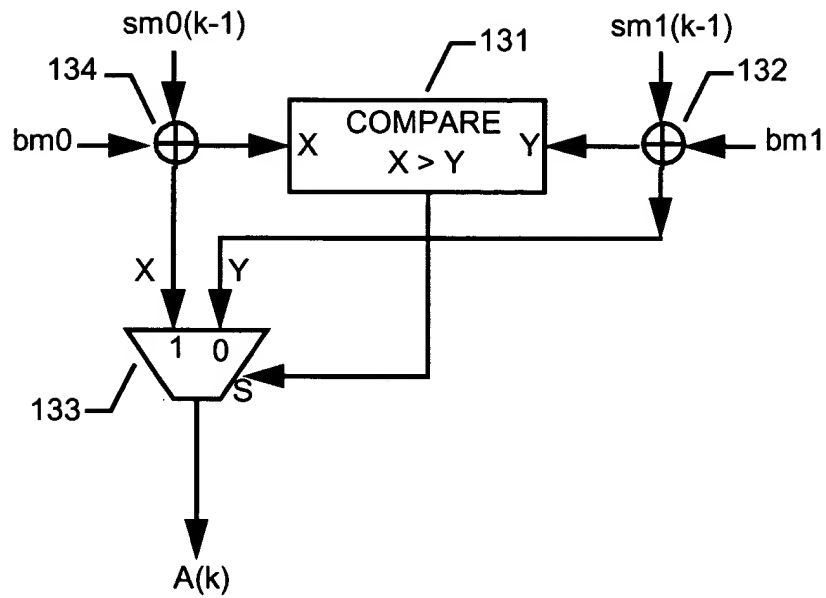


FIGURE 13. Computation of Forward Recursion of state-metric (ACS)



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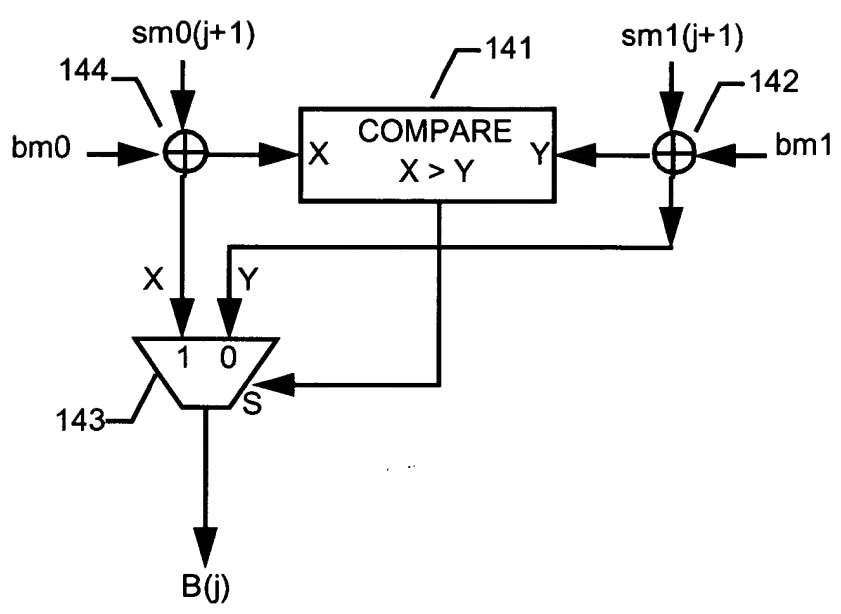


FIGURE 14. Computation of Backward Recursion of state-metric (ACS)

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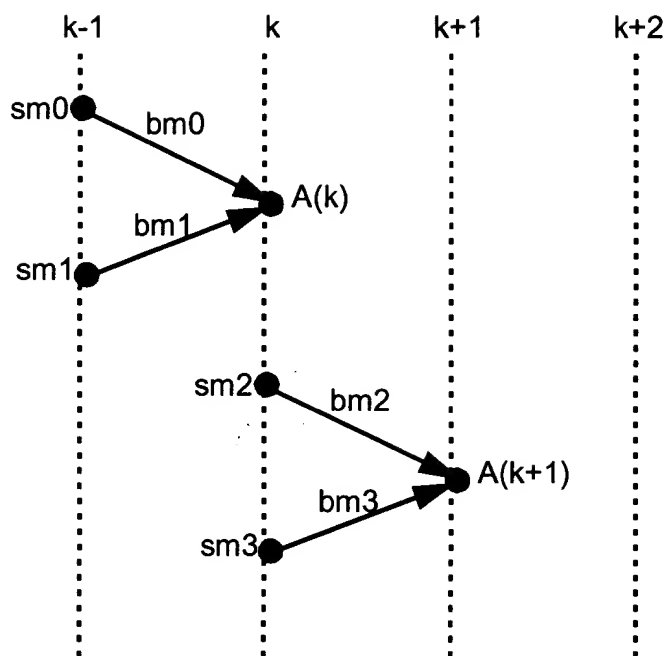
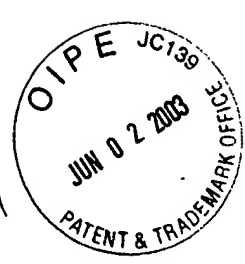


FIGURE 15. Forward computing of Trellis state transitions



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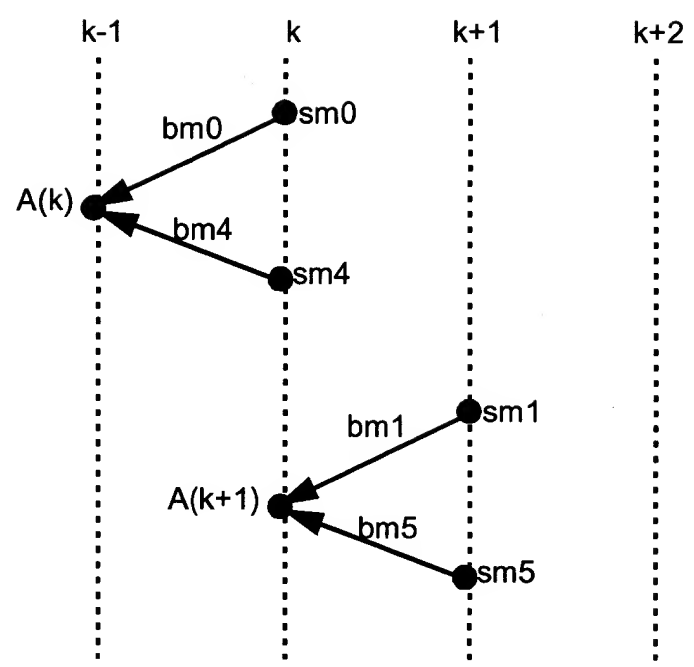


FIGURE 16. Backward computing of Trellis state transitions



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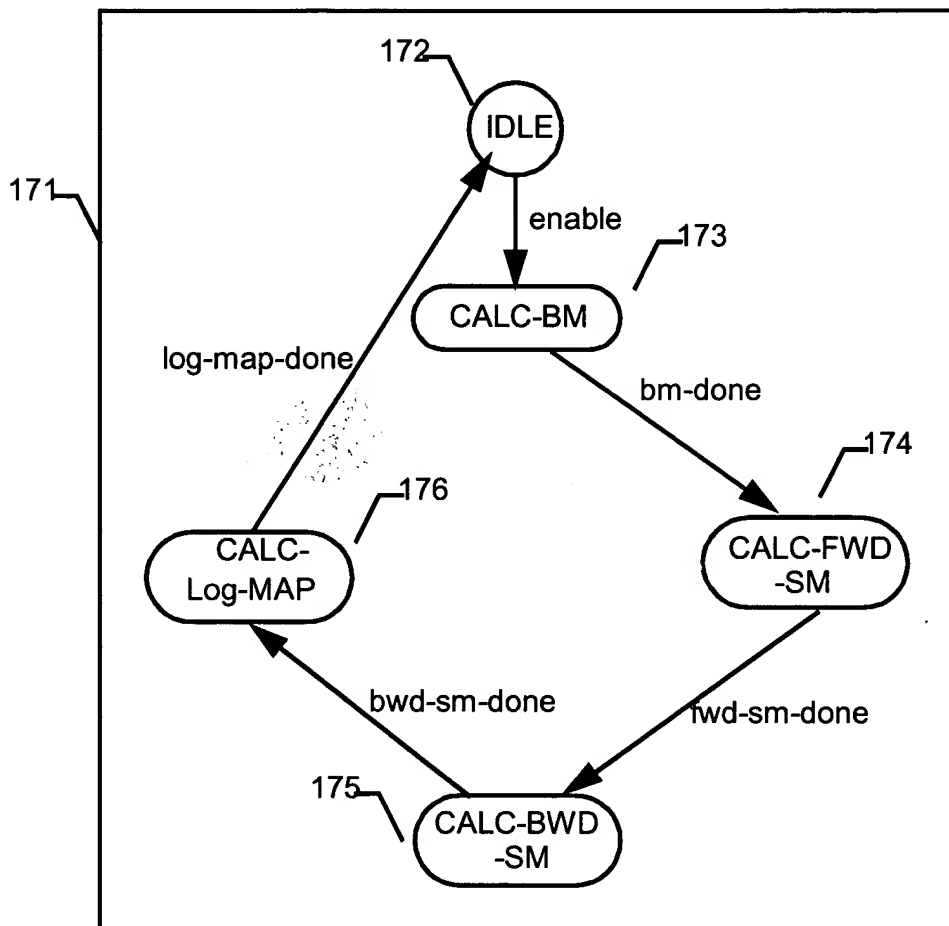


FIGURE 17. State machine operations of Log-MAP Decoder

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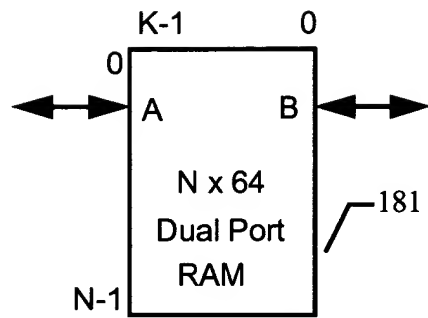


FIGURE 18. BM dual-port Memory Module

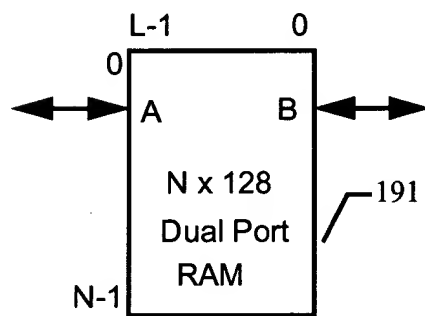
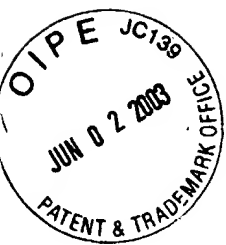


FIGURE 19. SM dual-port Memory Module



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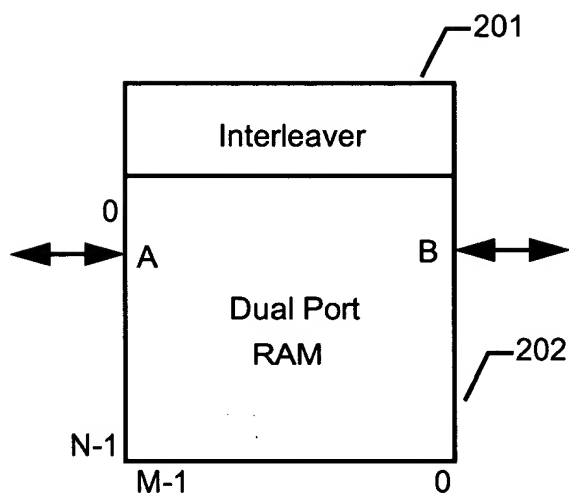


FIGURE 20. Interleaver RAM Memory Module

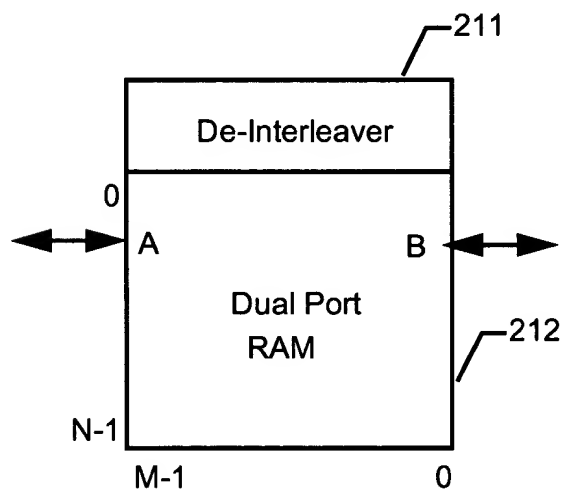
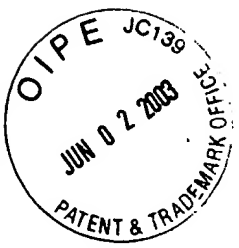


FIGURE 21. De-Interleaver RAM Memory Module



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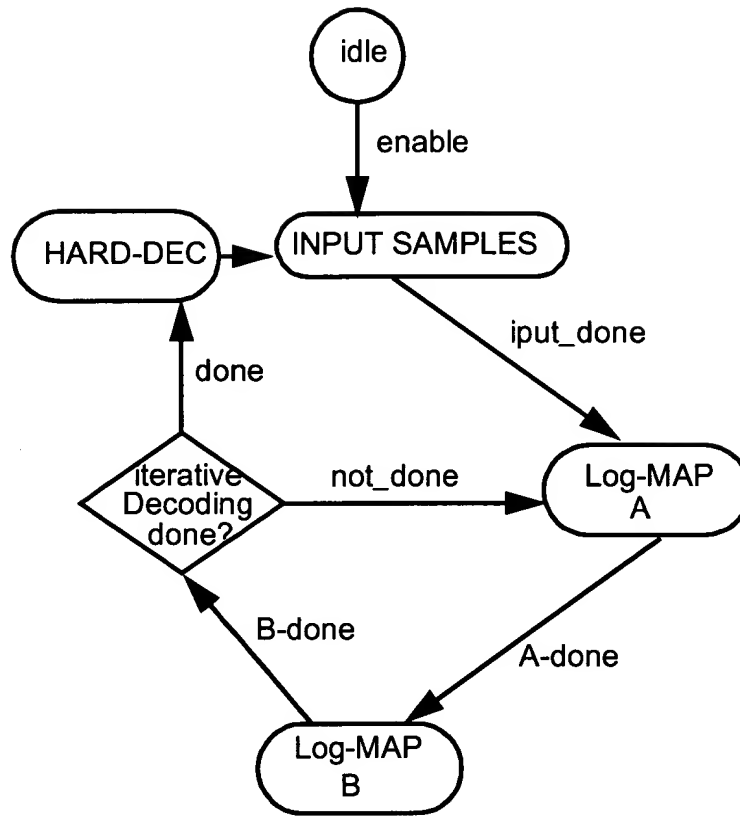


FIGURE 22. State machine operations of Turbo Decoder

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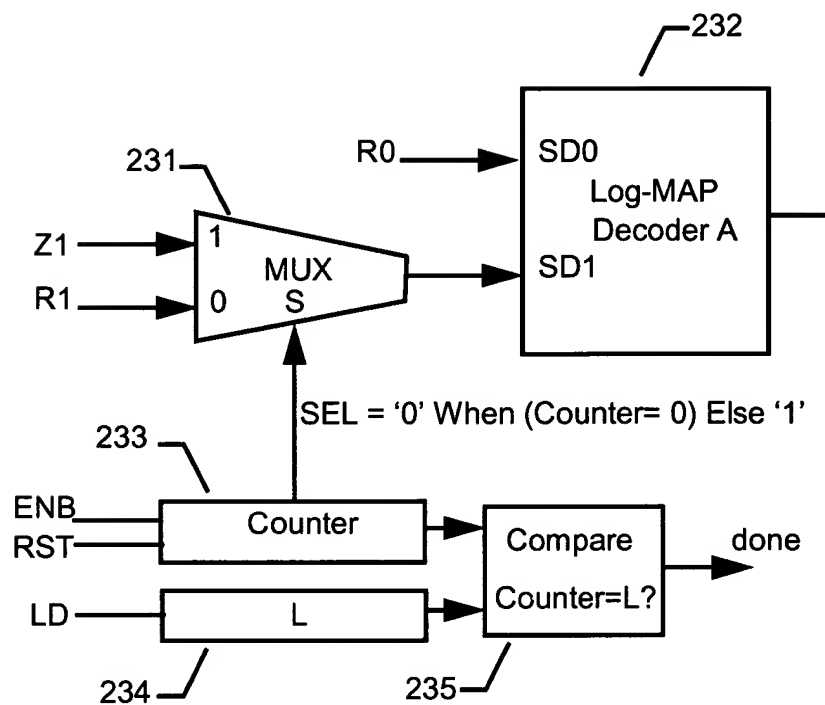


FIGURE 23. Iterative decoding feedback control Mux